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EXAMINER	
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ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,834	BLANC ET AL.	
	Examiner	Art Unit	
	Kibrom T. Hailu	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 5-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 9-25* is/are rejected.

7)☒ Claim(s) *2, 5-8, 10-13, 15 and 18-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed on August 08, 2007 have been fully considered but they are not persuasive because the cited reference discloses the rejected claims as set forth in the previous Office Action. The final rejections given below have been explained to provide more detail on how the claims are met by the cited reference of Shaikli (US 2003/0214949 A1). Therefore, the finality of this Office Action is deemed proper.

The arguments on page 12-15 of the Remarks are not persuasive, and thus claims are not patentable in view of the following disclosure.

Regarding claims 25, 9 and 12, the Applicants argue that Shaikli doesn't disclose, expressly or inherently, a CAM (Content Address Memory), and multicast data. First, CAM is simply a known associative memory, storage, array or table. And that is exactly what the Examiner indicated in the previous Office Action. The memory table 310 can be interpreted as CAM. If the Applicants are looking just for the name CAM, it is a well known name in the art. Even the Applicants admitted it is well known to those skilled in the art (please, see page 21, line 11 of the specification). Second the multicast data concept is well known in the art. Shaikli discloses a source, such as source processor A (can also call it ingress), distributes or multicasts a packet stream A through plurality of fabrics 1, 2 and 3 to at least one destination, such as destination processor D (see fig. 2). However, as indicated above, the multicast data concept is not novel. It is widely known concept.

Regarding claim 13, the Applicants argue that Shaikli doesn't disclose the "means" for numbering multicast packets. The Applicants assert that the table (401) indicated in figure 4 of

Shaikli doesn't correspond to the Applicants "means". However, if you carefully look at to figure 4 and its corresponding explanation, which is also cited by the Examiner (paragraph [0035], line 9-[0038]; [0008], lines 8-9), the packets are numbered according to priority or arrival time in table (401). Therefore, the Applicants argument is not persuasive.

Regarding claim 14, 21, 22, 23 and 25, the Applicants argue, "Shaikli does not disclose using a source identifier and priority level of the stored data packet to select or point to a corresponding-priority register that contains a packet sequence number and a packet buffer location identifier of a previously received data packet. Shaikli does show and teach four registers and table 310 as part of the reordering system. However, there are no clear teachings as to how a register is selected...."

The Examiner respectfully disagrees with the Applicants assertion because Shaikli discloses the argued limitation. First of all, as Shaikli shows, each of the packets has source identifier, priority information or level, packet sequence number and a memory pointer (or locator or buffer location identifier) associated with each of the packets (see paragraph [0041]; [0060], lines 7-10). Using this information, the source identifier and the priority information of the packet stored in the memory, the Enqueue logic 312 processes the sequence number and the memory or data pointer (Data_ptr) of the current and previous packet in the table 310 at the address pointed to by the register (See Fig. 6; paragraph [0061]; [0060], lines 7-10; [0059]; [0041]).

Claim Objections

1. Claims 2, 7, 10-13, 15, and 18-19 are objected to because of the following informalities:

Any limitation(s) within parentheses are not considered. It is unnecessary to put numbers in the claims while they are clearly shown in the specification and/or drawings. They created confusion with the numbers cited from the prior art reference. Applicants are advised to cancel the numbers in the parentheses.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite the limitation "the pointed source-priority register" on page 8, lines 4 and 18, respectively. There is insufficient antecedent basis for this limitation in the claims. Although the Examiner considered the words "select" and "point" as synonymous, consistent words have to be used. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 2 and 9-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shaikli (US 2003/0214949 A1).

Regarding claim 2, Shaikli discloses the first storing means (memory 306) comprise a free buffer list (401) to allocate a free packet buffer location (ID) to each received data packet (304) (paragraph [0047]).

Regarding claim 6, Shaikli discloses each of the plurality of source-priority registers (606, 608, 610 and 612) further comprise counting means (read pointer 606) to count for each sequence of data packets the number of data packets stored within said storing means waiting for being output from the at least one egress adapter (paragraphs [0064]; [0065], lines 12-19, ...the read pointer increments or counts to point to the next entry in the table to find the next sequenced packet to output).

Regarding claim 7, Shaikli discloses comprising scheduling means (dequeue logic 316) coupled to the CAM (memory table 310) and the plurality of source priority registers (Fig. 6, "the delay store registers", delay_store_register is just one example. The memory table 310 clearly shows the presence of plurality or delay store registers containing sequence numbers and memory or data pointers of the packets stored) for selecting one sequence of data packets from which a data packet is to be output from the at least one egress adapter (paragraphs [0009], lines 14-22; [0010], lines 12-14; [0047]).

Regarding claim 8, Shaikli discloses the scheduling means (dequeue logic 316) are coupled to the plurality of valid-bit latches (fig. 6, valid bits 630) to select one valid-bit latch among the valid-bit latches having their valid bit active (paragraph [0069], illustrates selecting "1" or "0" based on the validity of the bits).

Regarding claim 9, Shaikli discloses the received data packets comprise unicast and multicast data packets (see fig. 1, illustrates the packets are unicast and multicast packets. Note also that unicasting and multicasting are well known in the art).

Regarding claim 10, Shaikli discloses each of the plurality of ingress adapters comprise means (sequence encoder or encoder logic 202) for numbering the unicast data packets according to the priority level and to the at least one egress adapter of each unicast data packet (fig. 1 and 2; fig. 5, step 504; paragraphs [0021]; [0020], lines 4-6, explains the encoder logic or sequence encoder 202 of the source processors or ingresses assign sequence numbers to each packet according to their priority and the destination processor, which in this case destination processor D).

Regarding claim 11, Shaikli discloses each of the plurality of ingress adapters further comprises means for load balancing over a plurality of independent switching planes the numbered data packets (fig. 1; paragraph [0003], illustrates the numbered data packets are distributed or balanced to the plurality of the fabrics or switches to be switched to the intended destinations. Note also that since each of the numbered data packets are load balanced or distributed across the plurality of the switches, it is obvious for a person in the art to realize the presence of load balancer in each of the source processors or ingress adapters).

Regarding claim 12, Shaikli discloses each of the plurality of ingress adapters further comprises means for scheduling the switching of the unicast and multicast data packets over the plurality of independent switching planes (fig. 1; paragraphs [0008], lines 5-7; [0009], lines 7-9; [0010], lines 7-11).

Regarding claim 13, Shaikli discloses including at least one egress adapter (destination processor D) further comprises means (401) for numbering the multicast data packets according to the priority level of each multicast data packet and to the independent switching plane each multicast data packet has been switched through (fig. 1 and 4; paragraphs [0035], line 9-[0038]; [0008], line 18, explains the numbering or the reordering of the multicast data that are switched through each of the switching fabric based on the priority as well as other parameters, such as arrival time, transmitting sequence number and expiration time at the destination).

Regarding claim 14, Shaikli discloses a method for resequencing received data packets comprising for each received data packet (claim 11): allocating a packet buffer location to the received data packet and temporarily storing said received data packet at said allocated packet buffer location (paragraph [0025], lines 3-6; paragraph [0034], lines 1-3); using a source identifier and the priority level of the stored data packet to point to a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet (paragraphs [0041], [0054]-[0057], [0059], lines 4-9), the source-priority register being associated to a valid-bit latch that indicates an active or not active status (paragraph [0069]-[0070]); and checking the status of the valid-bit latch (paragraphs [0064], lines 6-11;[0065], lines 14-18) and comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet of the corresponding sequence of data packets (paragraphs [0066], line 4-10; [0067]-[0069]) .

Regarding claim 15, Shaikli discloses the checking step (paragraphs [0064], lines 6-11;[0065], lines 14-18) further comprises: if the status is not active (paragraph [0064], line 9, ...if the sequence number is not valid): updating the pointed source-priority register with the packet sequence number and the packet buffer location identifier of the received data packet, only if the packet sequence number of the received data packet is the next in sequence (paragraphs [0064], lines 9-[0065], lines 18, illustrates when the sequence number is not valid, i.e. if the packet is lost or time is expired, the read pointer register is incremented to the next entry in the table to find the next sequenced packet to output); and setting the status of the valid-bit latch to active (paragraph [0069]); otherwise, if the status is active (paragraph [0064], lines 6-7): writing in a Content Addressable Memory (memory table 310), the source identifier, the priority level and the packet sequence number of the received data packet, the write address being identified by the packet buffer location allocated to the received data packet (fig. 6, "table 310 and valid bits 630"; paragraphs [0064], lines 6-8; [0061], lines 3-13; [0055], lines 2-3; explains the parameters, sequence number, priority and identifier, are written into the table).

Regarding claim 16, Shaikli further discloses comprising incrementing a `waiting packet` counter (paragraph [0065], lines 8-14, the read pointer register is incremented to point to the next in the table to find the next sequenced packet to output).

Regarding claim 17, Shaikli further discloses comprising the scheduling the output of the received data packet from the at least one egress adapter (paragraph [0064], lines 6-8, illustrates when the value read from the table at the selected sequence number is valid, the data is retrieved from the memory for output).

Regarding claim 18, Shaikli further discloses comprising the step of decrementing the `waiting packet` counter after transmitting the received data packet (paragraph [0047], explains when a packet is unloaded or outputted from the memory, the memory gets empty to store newly arrived data packets, and the memory pointer associated with the packet is reused.... Thus, it is obvious to say that the memory pointer is decreased when a packet is unloaded from memory for output).

Regarding claim 19, Shaikli discloses searching the Content Addressable Memory (table 310) for the next packet sequence number (fig. 6; paragraph [0066], lines 1-4); and if the search match (fig. 6; paragraph [0066], lines 6-7, when the read_ptr equals the current value sequence number): updating the source-priority register with the founded next packet sequence number and the corresponding packet buffer location identifier (fig. 6; paragraph [0066], lines 4-7, illustrates the current_value register is updated when the read_ptr equals the current value sequence number, and the corresponding packet buffer location identifier, such as data_ptr_20 corresponds to the sequence number 20); keeping the status of the valid-bit latch to active (paragraph [0069], lines 7-8); and invalidating the searched CAM entry (paragraph [0069], lines 1-4); otherwise, if the search does not match, resetting the status of the valid-bit latch of the pointed source-priority register (paragraph [0069], lines 4-12).

Regarding claim 20, Shaikli further discloses comprising after the resetting starting a timer (paragraph [0065], lines 10-18).

Regarding claim 21, Shaikli discloses a system (abstract) comprising: a buffer in which received data packets are temporarily stored (paragraph [0025], lines 3-6; [0034], lines 1-3); a controller programmed to use the source identifier and the priority level of the stored data packet

to select a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet, the source-priority register being associated with a valid-bit latch that indicates an active/not active status (paragraphs [0041]; [0054]-[0057]; [0059], lines 4-9; [0042]; [0047], lines 4-6); and said controller programmed to check the status of the valid-bit latch (paragraphs [0064], lines 6-11; [0065], lines 14-18) and comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet in the corresponding sequence of data packets (paragraphs [0066], line 4-10; [0067]-[0069]).

Regarding claim 22, Shaikli discloses a computer program product comprising: a computer readable medium containing computer readable code including a first instruction module for accessing a buffer in which received data packets are temporarily stored (paragraph [0025], lines 3-6; [0034], lines 1-3) and to use a source identifier and the priority level of the stored data packet to select a corresponding source-priority register that contains a packet sequence number (PSN) and a packet buffer location identifier (ID) of a previously received data packet, the source-priority register being associated to a valid-bit latch that indicates an active or not active status (paragraphs [0041]; [0054]-[0057]; [0059], lines 4-9; [0042]; [0047], lines 4-6); and a second instruction module to check the status of the valid-bit latch (paragraphs [0064], lines 6-11; [0065], lines 14-18) and comparing the packet sequence number of the received data packet with the packet sequence number contained within the pointed source-priority register to determine if the received data packet is to be output as the next data packet of the corresponding sequence of data packets (paragraphs [0066], line 4-10; [0067]-[0069]).

Regarding claim 23, Shaikli discloses a method comprising: a) providing a buffer in which packets exiting a device is temporarily stored (paragraph [0025], lines 3-6; paragraph [0034], lines 1-3); b) providing at least one source priority register identifying at least one packet by at least Source Priority (S.sub.1, P.sub.1-n,), Packet Serial No. (PSN) and location of packet in said buffer (ID) (paragraphs [0041]; [0054]-[0057]; [0059], lines 4-9; [0042]; [0047], lines 4-6); c) providing at least one validity latch (630, "v1 and v2, valid bits) whose setting indicates status of said at least one packet (paragraph [0069]-[0070]); and d) scheduling a packet for transmission based upon state of the validity latch (paragraph [0064], lines 6-8, illustrates when the value read from the table at the selected sequence number is valid, the data is retrieved from the memory for output).

Regarding claim 24, Shaikli discloses including repeating d) so long as another packet having a packet sequence number in-sequence with a last scheduled packet is found in the buffer (paragraphs [0044]; [0047], lines 6-10; [0064], lines 1-6; [0071], lines 5-9; [0090], lines 8-10).

Regarding claim 25, Shaikli discloses system for resequencing received data packets comprising (Abstract):

a first means (memory 306) for storing each received data packet at an allocated location within said first means (paragraph [0025], lines 3-6; paragraph [0034], lines 1-3); a Content Address Memory (CAM) (memory table 310) having at least one entry comprising an identification field (memory pointer 604) to contain a packet buffer identifier (ID) field to identify an allocated location in said first means whereat a received data packet is placed, a search field to contain a source identifier of a source providing said receive data packet (paragraphs [0042]; [0047], lines 4-6), a priority level for said receive data packet and a

sequence number for said receive data packet, wherein recited fields are concatenated (paragraphs [0042]; [0047], lines 4-6), and a search field to contain the source identifier, the priority level and the packet sequence number of each stored data packet (paragraph [0041], lines 1-3); a plurality of source-priority registers each containing, a packet sequence number (PSN) and a packet buffer identifier (ID) of a data packet previously transmitted from said first means (Fig. 6; paragraph [0059], lines 4-9; [0061], shows the memory table 310 contains plurality of delay-store-registers containing sequence numbers and memory or data pointers, such as Data_ptr_5, Data_ptr_7, Data_ptr_10 and so on); and a plurality of valid-bit latches respectively associated to the plurality of source priority registers to set an active status to indicate that corresponding stored data packet is the next one in sequence (see Fig. 6; paragraphs [0064], lines 6-11; [0065], lines 14-18; [0066], line 4-10; [0067]-[0069]).

Allowable Subject Matter

6. Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior of arts of record do not teach or suggest, "the number of source-priority registers and associated valid-bit latches are equal to the number of sources providing packets multiply by number o priority levels" as amended to claim 5.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom T. Hailu whose telephone number is (571)270-1209. The examiner can normally be reached on Monday-Thursday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571)272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KTH
12/05/07

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SUPERVISORY PATENT EXAMINER